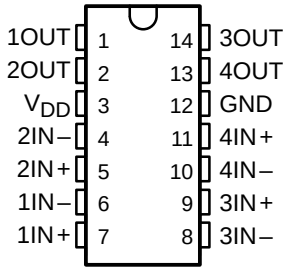
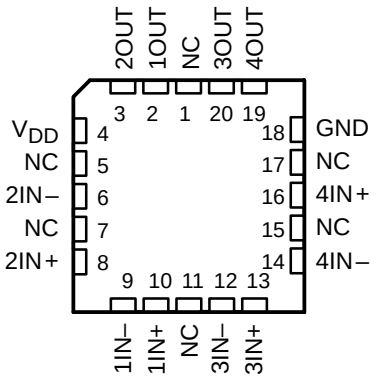
- **Single- or Dual-Supply Operation**
- **Wide Range of Supply Voltages 2 V to 18 V**
- **Very Low Supply Current Drain 0.3 mA Typ at 5 V**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible With TTL, MOS, and CMOS**
- **Pin-Compatible With LM339**

D, J, N, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)

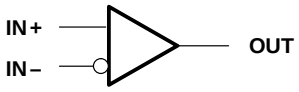


NC – No internal connection

description

These quadruple differential comparators are fabricated using LinCMOS™ technology and consist of four independent voltage comparators designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 2 V to 18 V. Each device features extremely high input impedance (typically greater than 10^{12} Ω), allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships.

symbol (each comparator)



The TLC374 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 1000-V ESD rating using human body model testing. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC374C is characterized for operation from 0°C to 70°C. The TLC374I is characterized for operation from –40° to 85°C. The TLC374M is characterized for operation over full military temperature range of –55°C to 125°C. The TLC374Q is characterized for operation from –40°C to 125°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . V_{DD}
Input voltage range, V_I . . . . . –0.3 V to 18 V
Output voltage, V_O . . . . . 18 V
Input current, I_I . . . . . ±5 mA
Output current, I_O . . . . . 20 mA
Duration of output short circuit to ground (see Note 3) . . . . . unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC374C . . . . . 0°C to 70°C
TLC374I . . . . . –40°C to 85°C
TLC374M . . . . . –55°C to 125°C
TLC374Q . . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature range for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, N, or PW package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN –.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	7.6 mW/°C	84°C	500 mW	494 mW	190 mW
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	269 mW
J	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	269 mW
N	500 mW	9.2 mW/°C	95°C	500 mW	500 mW	224 mW
PW	700 mW	5.6 mW/°C	—	448 mW	—	—

recommended operating conditions

		TLC374C		TLC374I		TLC374M		TLC374Q		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	3	16	4	16	3	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0	3.5	0	3.5	0	3.5	0	3.5	V
	V_{DD} = 10 V	0	8.5	0	8.5	0	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	–40	85	–55	125	–40	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC374C			TLC374I			TLC374M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 4		25°C		1	5		1	5		1	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			0 to $V_{DD}-1$			0 to $V_{DD}-1$			V
				Full range	0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = –1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 1 V,	No load	25°C		300	600		300	600		300	600	µA
				Full range			800			800			800	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC374C, –40°C to 85°C for TLC374I, and –55°C to 125°C for the TLC374M, and –40°C to 125°C for TLC374Q. MAX is 70°C for TLC374C, 85°C TLC374I, and 125°C for the TLC374M, and 125°C for TLC374Q. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLC374C, TLC374I TLC374M, TLC374Q			UNIT
			MIN	TYP	MAX	
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC374Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min,	See Note 4		1	5	mV
I_{IO}	Input offset current				1		pA
I_{IB}	Input bias current				5		pA
V_{ICR}	Common-mode input voltage range			0 to V_{DD}–1			V
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 5 V		0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 4 mA		150	400	mV
I_{OL}	Low-level output current	V_{ID} = –1 V,	V_{OL} = 1.5 mV	6	16		mA
I_{DD}	Supply current (four comparators)	V_{ID} =1 V,	No load		300	600	µA

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLC374Y			UNIT
			MIN	TYP	MAX	
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF†, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

† C_L includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PRINCIPLES OF OPERATION

LinCMOS process

LinCMOS process is a linear polysilicon-gate complimentary-MOS process. Primarily designed for single-supply applications, LinCMOS products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS products. Further questions should be directed to the nearest TI field sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g. during board assembly. If a circuit in which one amplifier from a dual operational amplifier is being used and the unused pins are left open, high voltages tends to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 4. This circuit can withstand several successive 1-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of TI's ESD-protection circuit is presented on the next page.

All input an output pins of LinCMOS and Advanced LinCMOS products have associated ESD-protection circuitry that undergoes qualification testing to withstand 1000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

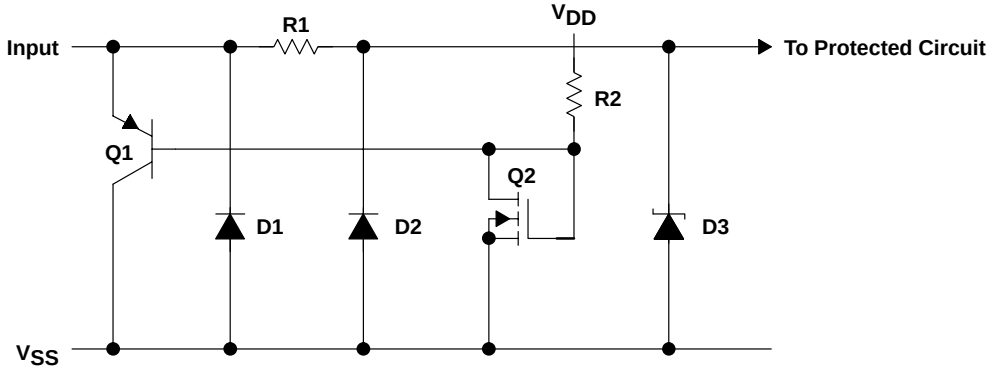


Figure 4. LinCMOS ESD-Protection Schematic

PRINCIPLES OF OPERATION

Input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 turns on when the voltage at the input rises above the voltage on V_{DD} by a value equal to the V_{EB} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 as Q1 saturates forces the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn on Q2. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of d3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 V to 27 V, which is well below the gate oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward-biased. The voltage seen by the protected circuit is –0.3 V to –1 V (the forward voltage of D1 and D2).

circuit-design considerations

LinCMOS products are being used in actual circuits environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figures 5 and 6 show typical characteristics for input voltage vs input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. The input current should be externally limited even through internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limits the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 5. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2, and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 7).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-87659012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-8765901CA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
TLC374CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC374CDB	ACTIVE	SSOP	DB	14	80	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TLC374CDBR	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TLC374CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC374CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPD	Level-NC-NC-NC
TLC374CN-A	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPD	Level-NC-NC-NC
TLC374CN-AE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPD	Level-NC-NC-NC
TLC374CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPD	Level-NC-NC-NC
TLC374CNSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TLC374CPW	ACTIVE	TSSOP	PW	14	90	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC374CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
TLC374CPWR	ACTIVE	TSSOP	PW	14	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC374ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC374IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC374IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPD	Level-NC-NC-NC
TLC374INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPD	Level-NC-NC-NC
TLC374MD	ACTIVE	SOIC	D	14	50	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC374MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TLC374MJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
TLC374MJB	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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