L4995

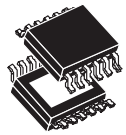
5V, 500mA low drop voltage regulator

Features

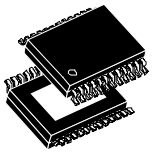
Max DC supply voltage	V_S	40V
Max output voltage tolerance	ΔV_0	+/-2%
Max dropout voltage	V_{dp}	500mV
Output current	I_0	500mA
Quiescent current	I_{qn}	3µA(1)

1. Typical value with regulator disabled

- Operating DC supply voltage range 5.6V to 31V
- Low dropout voltage
- Low quiescent current consumption
- Reset circuit sensing of output voltage down to 1V
- Programmable reset pulse delay with external capacitor
- Programmable watchdog(a) timer with external capacitor
- Thermal shutdown and short circuit protection
- Wide temperature range (T_j = -40°C to 150°C)
- Enable(a) input for enabling / disabling the voltage regulator



PowerSSO-12



PowerSSO-24

Description

L4995 is a family of monolithic integrated 5V voltage regulators with a low drop voltage at currents of up to 500mA, available in both 12 and 24 pin packages.

The output voltage regulating element consists of a p-channel MOS and regulation is performed regardless of input voltage transients of up to 40V. The high precision of the output voltage is obtained using a pre-trimmed reference voltage. The L4995 family is protected against short circuit and over-temperature protection switches off the devices in the case of extremely high power dissipation.

- The L4995 integrates the Watchdog, Enable and externally programmable Reset circuits.
- The L4995A features the externally programmable Reset and Enable.
- Finally the L4995R features the externally programmable Reset.

The combination of such features makes this device particularly flexible and suitable to supply microprocessor systems in automotive applications.

Table 1. Device summary

Package	Order codes	
	Tube	Tape & reel
PowerSSO-12 (exposed pad)	L4995J - L4995AJ - L4995RJ	L4995JTR - L4995AJTR - L4995RJTR
PowerSSO-24 (exposed pad)	L4995K - L4995AK - L4995RK	L4995KTR - L4995AKTR - L4995RKTR

P/N	Watchdog	Reset	Enable
L4995J - L4995K	X	X	X
L4995AJ - L4995AK	-	X	X
L4995RJ - L4995RK	-	X	-

a. Watchdog and Enable facilities are available according to *Table 1: Device summary*

Contents

List of tables

List of figures

1 Block diagrams and pins descriptions

Figure 1. Block diagram of L4995

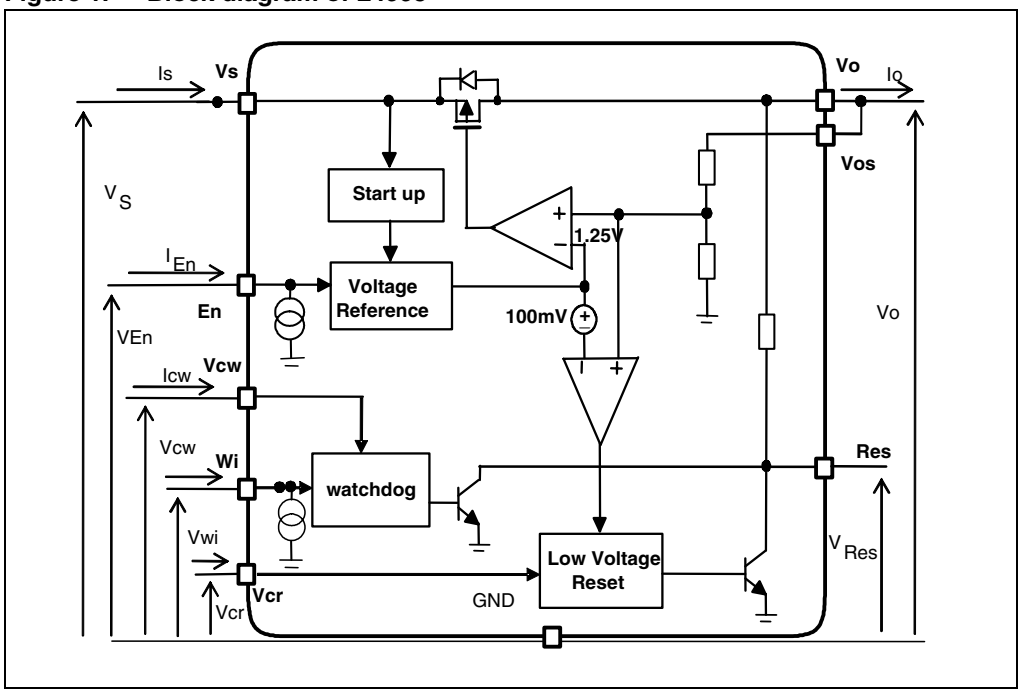


Figure 2. Block diagram of L4995A

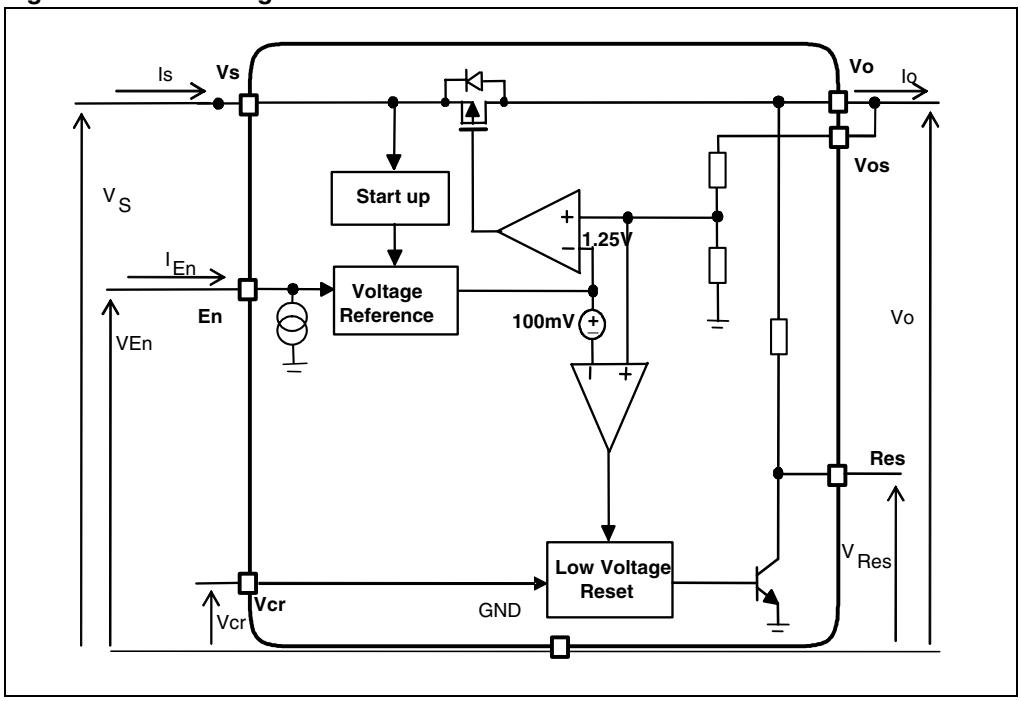


Figure 3. Block diagram of L4995R

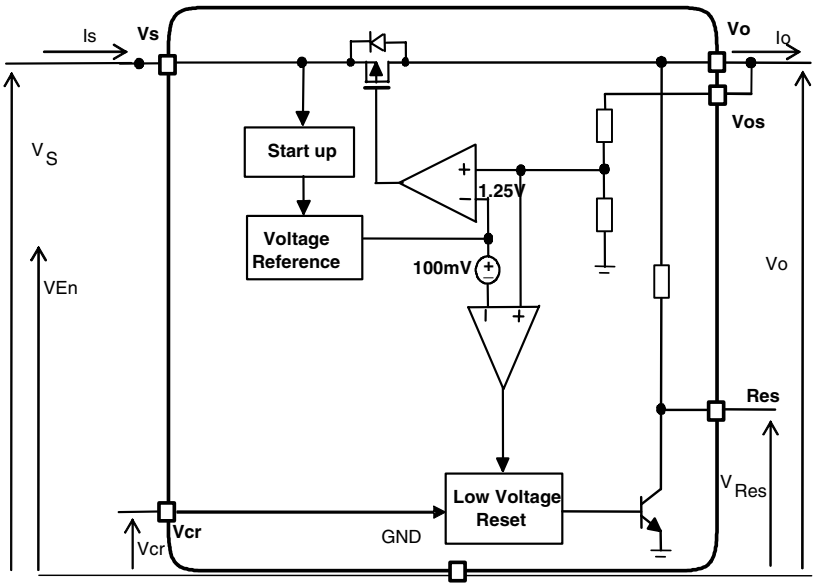


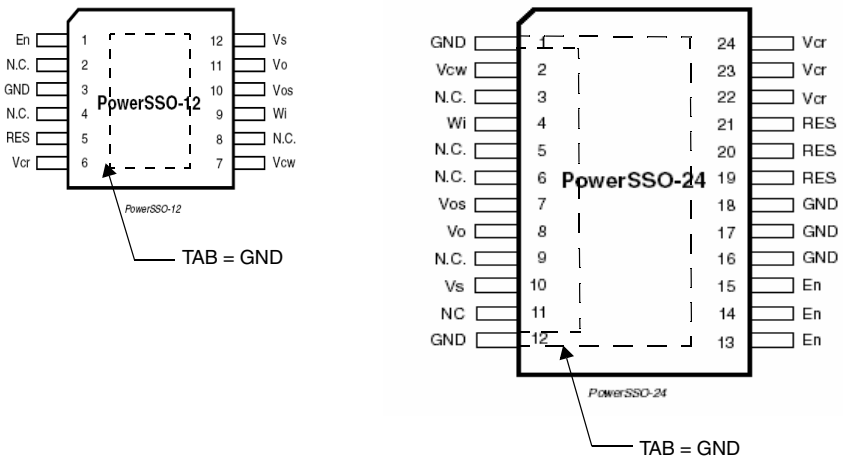
Table 2. Pins descriptions

Pin name	PowerSSO-12 pin #	PowerSSO-24 pin #	Function
En	1	13, 14, 15	Enable input (L4995 and L4996A only, otherwise not connected). If high regulator, watchdog and reset are operating. If low regulator, watchdog and reset are shut down. Connect to Vs if not used.
NC	2, 4, 8	3, 5, 6, 9, 11	Not connected.
Gnd	3	16, 17, 18	Ground reference.
Gnd	-	1, 12	Ground (these pins are to be connected to a heat spreader electrically grounded).
Res	5	19, 20, 21	Reset output. It is pulled down when output voltage goes below Vo_th or frequency at Wi is too low. Leave floating if not used.
Vcr	6	22, 23, 24	Reset timing adjust. A capacitor between Vcr pin and gnd. sets the reset delay time (trd). Leave floating if Reset is not used.
Vcw	7	2	Watchdog timer adjust (L4995 only, otherwise not connected). A capacitor between Vcw pin and gnd. sets the time response of the watchdog monitor.

Table 2. Pins descriptions (continued)

Pin name	PowerSSO-12 pin #	PowerSSO-24 pin #	Function
Wi	9	4	Watchdog input (L4995 only, otherwise not connected). If the frequency at this input pin is too low, the Reset output is activated.
Vo_s	10	7	Regulator voltage output sensing.
Vo	11	8	5 voltage regulator output. Block to ground with a capacitor >100nF (needed for regulator stability).
Vs	12	10	Supply voltage. Block to ground directly at Vs pin with a ceramic capacitor (e.g. 200nF).

Figure 4. Pins configurations (L4995)



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{Vsdc}	DC supply voltage	- 0.3 to 40	V
I_{Vsdc}	Input current	Internally limited	
V_{Vo}	DC output voltage	- 0.3 to 6	V
I_{Vo}	DC output current	Internally limited	
V_{Wi}	Watchdog input voltage	-0.3 to V_{Vo} + 0.3	V
V_{od}	Res output voltage	-0.3 to V_{Vo} + 0.3	V
I_{od}	Res output current	Internally limited	
V_{cr}	Vcr voltage	- 0.3 to V_{Vo} + 0.3	V
V_{cw}	Watchdog delay voltage	- 0.3 to V_{Vo} + 0.3	V
V_{En}	Enable input	- 0.3 to V_{Vsdc} +0.3	V
T_j	Junction temperature	- 40 to 150	C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	± 2	kV
V_{ESD}	ESD voltage level (CDM AEC-Q100-011)	750	V

2.2 Thermal data

For details, please refer to *Section 4.1: PowerSSO-12™ thermal data* and *Section 4.2: PowerSSO-24™ thermal data*.

Table 4. Thermal data(1)

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance Junction to Ambient: PowerSSO-12 PowerSSO-24	 5 4	 °K/W °K/W
$R_{thj\text{-}amb}$	Thermal resistance Junction to Ambient: PowerSSO-12 PowerSSO-24	 52 38	 °K/W °K/W

1. The values quoted are for PCB 77mm x 86mm x 1.6mm, FR4, double layer; Copper thickness 0.070mm Copper area 3cm2 Thermal Vias, Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm.

2.3 Electrical characteristics

Values specified in this section are for V_s = 5.6V to 31V, T_j = -40 °C to +150 °C unless otherwise stated.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Vo	V_{o_ref}	Output voltage	Vs = 5.6 to 31V Io = 0 to 500mA	4.9	5.00	5.1	V
Vo	I_{short}	Short circuit current	Vs = 13.5V (1)	550	800	1050	mA
Vo	I_{lim}(2)	Output current limitation	Vs = 13.5V (1)	600	900	1250	mA
Vs, Vo	V_{line}	Line regulation voltage	Vs = 5.6 to 31V Io = 0 to 500mA			25	mV
Vo	V_{load}	Load regulation voltage	Io = 0 to 500mA			25	mV
Vs, Vo	V_{dp}(3)	Drop voltage	Io = 400mA		270	500	mV
Vs, Vo	SVR	Ripple rejection	fr = 100 Hz (4)	55			dB
Vs, Vo	I_{qs}	Current consumption with regulator disabled	Vs = 13.5V, En = low		3	10	µA
Vs, Vo	I_{qn_1}	Current consumption with regulator enabled	Vs = 13.5V, Io < 1mA,		90	160	µA
Vs, Vo	I_{qn_50}	Current consumption with regulator enabled	Vs = 13.5V, Io = 50mA,		290	400	µA

Table 5. General (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Vs, Vo	I_{qn_150}	Current consumption with regulator enabled	Vs = 13.5V, Io = 150mA,		740	1000	µA
Vs, Vo	I_{qn_250}	Current consumption with regulator enabled	Vs= 13.5V, Io= 250mA,		1	1.4	mA
Vs, Vo	I_{qn_500}	Current consumption with regulator enabled	Vs= 13.5V, Io= 500mA,		2.1	2.7	mA
	Tw	Thermal protection temperature		150		190	°C
	Tw_hy	Thermal protection temperature hysteresis			10		°C

1. See *Figure 27*.
2. Measured output current when the output voltage has dropped 100mV from its nominal value obtained at Vs=13.5V and Io= 250mA.
3. Vs-Vo measured when the output voltage has dropped 100mV from its nominal value obtained at Vs=13.5V and Io= 250mA.
4. Guaranteed by design.

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Res	Vres_l	Reset output low voltage	R_{ext} = 5kΩ to Vo, Vo > 1V			0.4	V
Res	I_{Res_lkg}	Reset output high leakage current	V_{Res} = 5V			1	µA
Res	R_{Res}	Pull up internal resistance (versus Vo)		10	20	40	kΩ
Res	Vo_th	Vo out of regulation threshold	Vs = 5.6 to 31V Io = 1 to 500mA	6%	8%	10%	below V_{o_ref}
Vcr	Vrlth	Reset delay circuit low threshold	Vs = 13.5V	10%	13%	16%	V_{o_ref}
Vcr	Vrhth	Reset delay circuit high threshold	Vs =13.5V	44%	47%	50%	V_{o_ref}
Vcr	Icr	Charge current	Vs = 13.5V	8	15	30	µA
Vcr	Idr	Discharge current	Vs = 13.5V	8	15	30	µA
Res	Trr	Reset reaction time(1)	Vo = V_{o_th} -100mV	100	250	700	µs
Res	Trd	Reset delay time	Vs = 13.5V, Ctr = 47nF	13	39	70	ms

1. When Vo becomes lower than 4V, the reset reaction time decreases down to 2µs assuring a faster reset condition in this particular case.

Table 7. Watchdog

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Wi	Vih	Input high voltage	Vs = 13.5V	3.5			V
Wi	Vil	Input low voltage	Vs = 13.5V			1.5	V
Wi	Vih	Input hysteresis	Vs = 13.5V		500		mV
Wi	Iwi	Pull down current	Vs = 13.5V Vwi = 3.5V		6	10	µA
Vcw	Vwlth	Low threshold	Vs = 13.5V	10%	13%	16%	V_{o_ref}
Vcw	Vwhth	High threshold	Vs = 13.5V	44%	47%	50%	V_{o_ref}
Vcw	Icwc	Charge current	Vs = 13.5V, Vcw = 0.1V	5	10	20	µA
Vcw	Icwd	Discharge current	Vs = 13.5V, Vcw = 2.5V	1.25	2.5	5	µA
Vcw	Twop	Watchdog period	Vs = 13.5V, Ctw = 47nF	20	40	80	ms
Res	twol	Watchdog output low time	Vs = 13.5V, Ctw = 47nF	4	8	16	ms

Table 8. Enable

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
En	V_{En_low}	En input low voltage				1	V
En	V_{En_high}	En input high voltage		3			V
En	V_{En_hyst}	En input hysteresis			830		mV
En	I_{En}	Pull down current	Vs = 13.5V		10	18	µA

2.4 Electrical characteristics curves

Figure 5. Output voltage vs. Tj

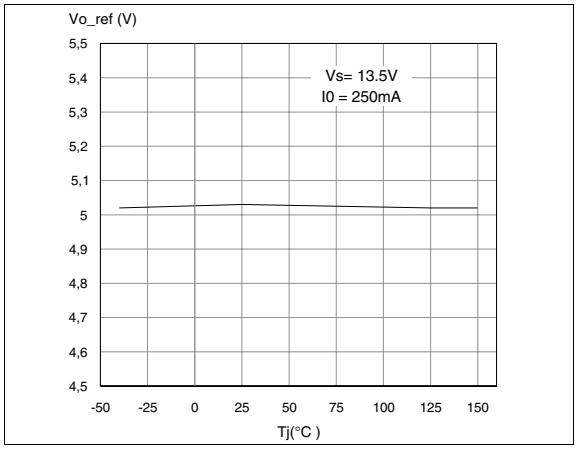


Figure 6. Output voltage vs. Vs

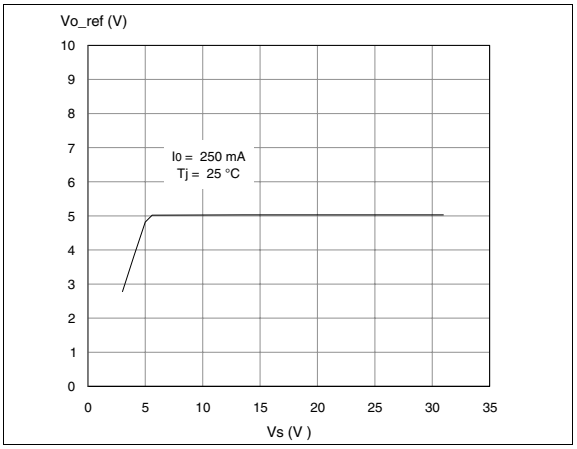


Figure 7. Drop Voltage vs. Output Current

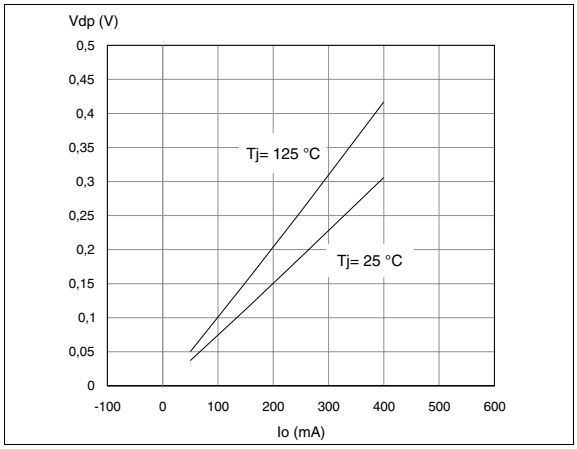


Figure 8. Current consumption vs. Output Current

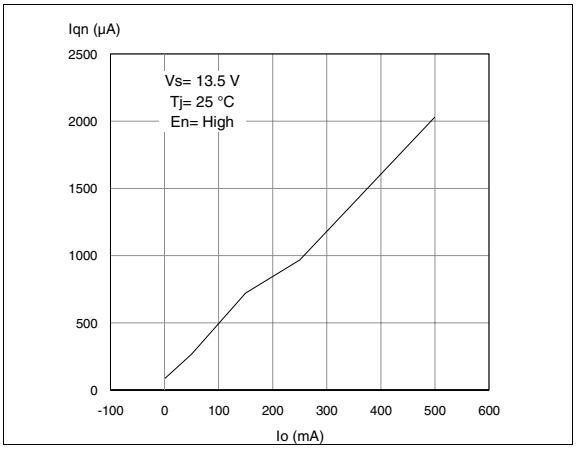


Figure 9. Current consumption vs. Input Voltage

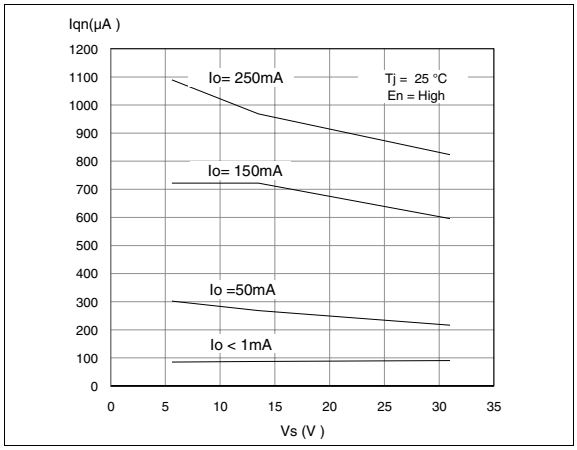


Figure 10. Current limitation vs. Tj

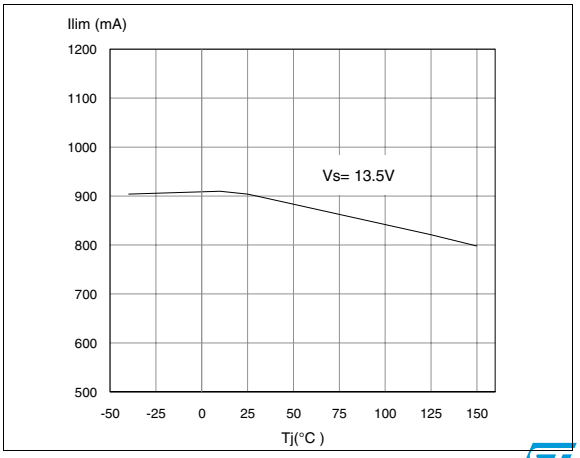


Figure 11. Current limitation vs. Input Voltage

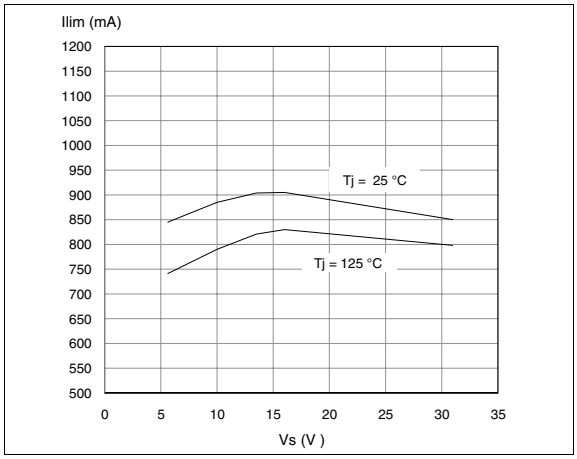


Figure 12. Short Circuit Current vs. Input Voltage

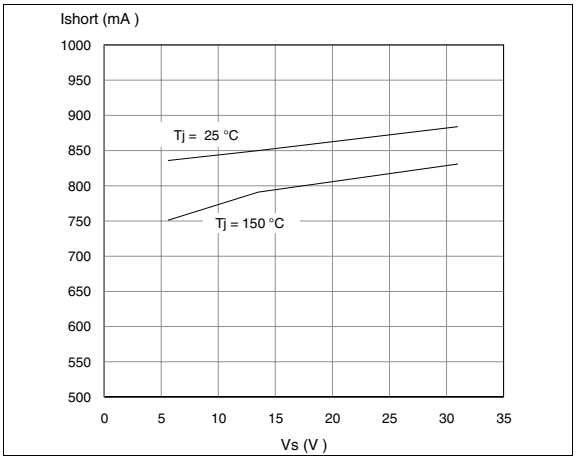


Figure 13. Output Voltage vs. Enable Voltage

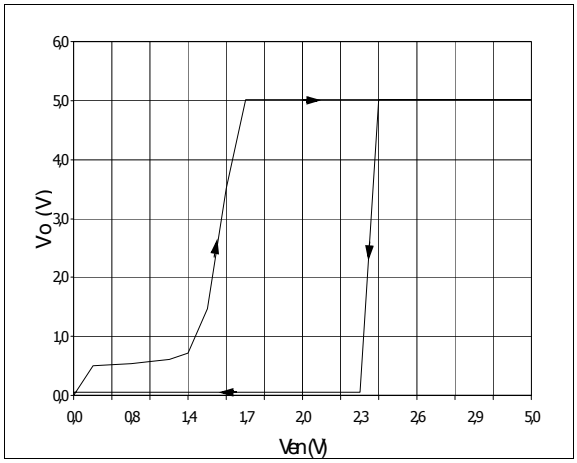


Figure 14. V_{En_high} vs. Tj

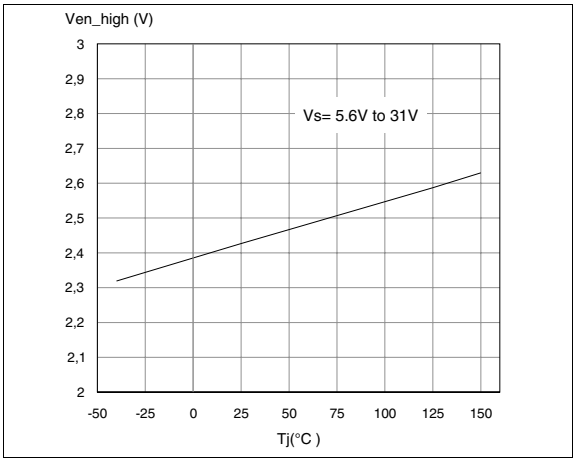


Figure 15. V_{EN_LOW} vs. Tj

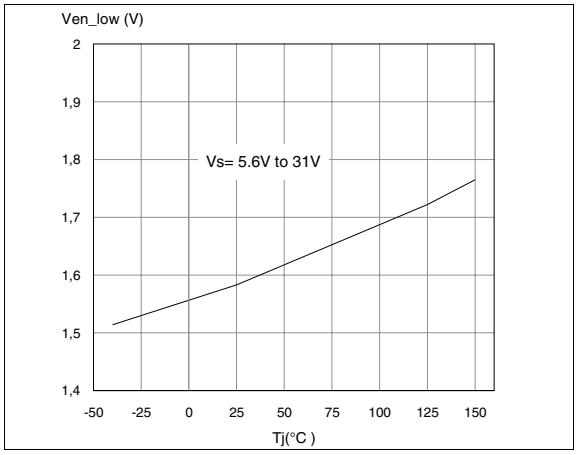


Figure 16. Vrhth vs. Tj

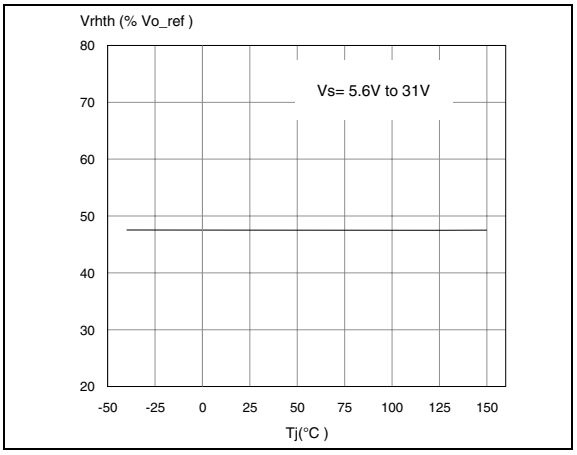


Figure 17. Vrlth vs. Tj

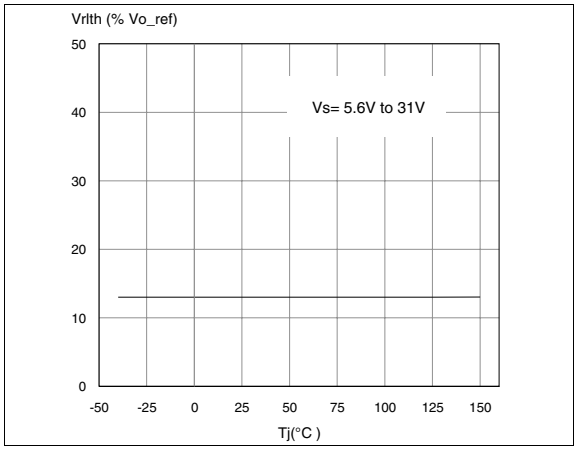


Figure 18. Vwhth vs. Tj

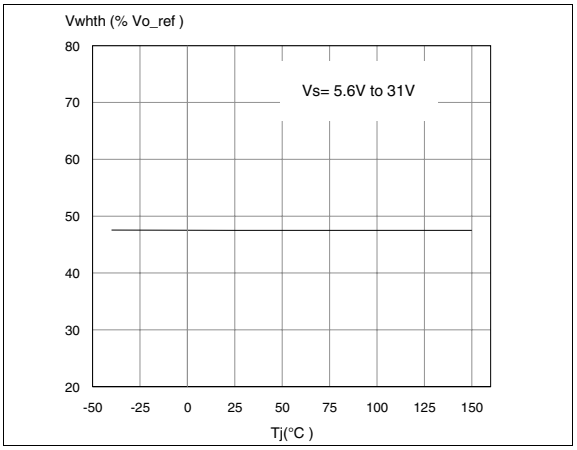


Figure 19. Vwlth vs. Tj

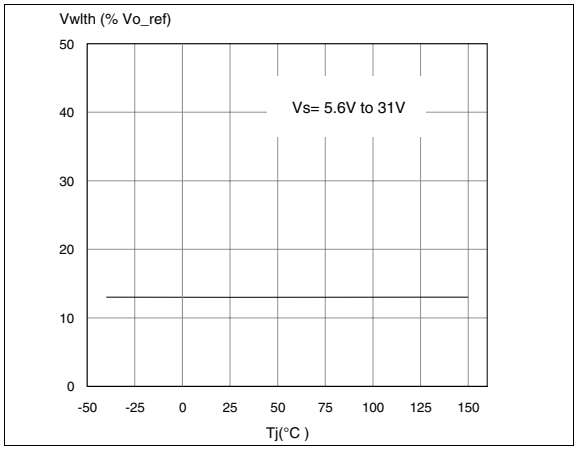


Figure 20. Icr & Icwc vs. Tj

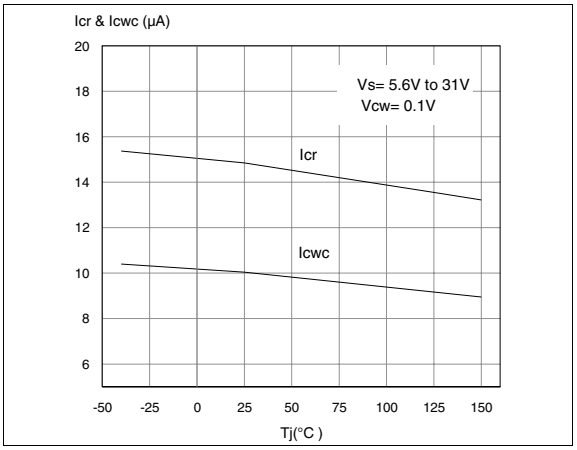


Figure 21. Idr & Icwd vs. Tj

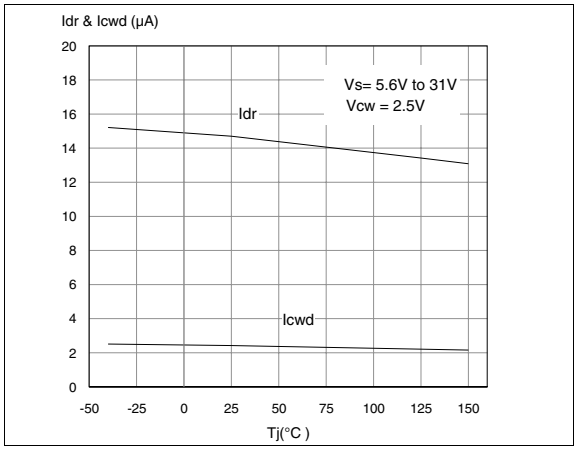


Figure 22. Twop vs. Tj

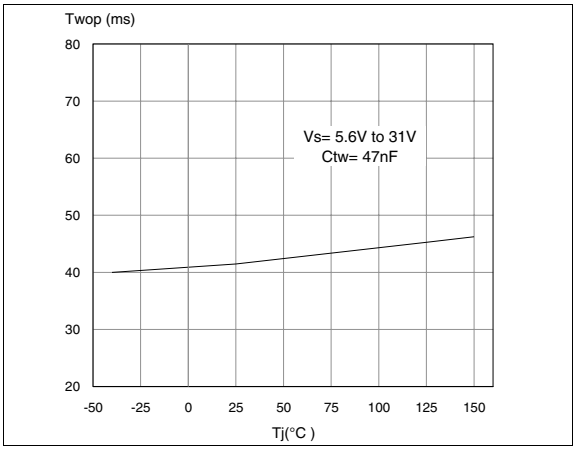
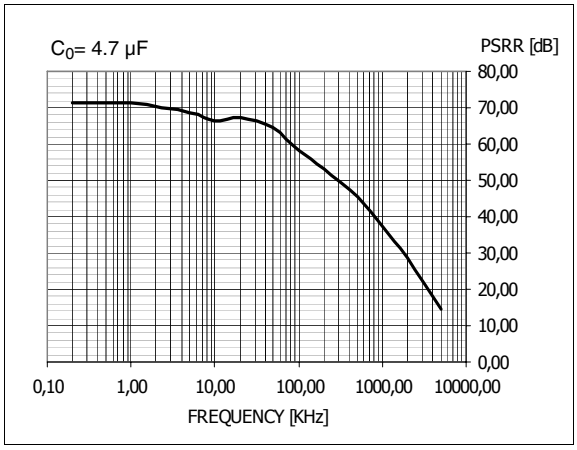


Figure 23. PSRR



2.5 Test circuit and waveforms plot

2.5.1 Load regulation

Figure 24. Load regulation test circuit

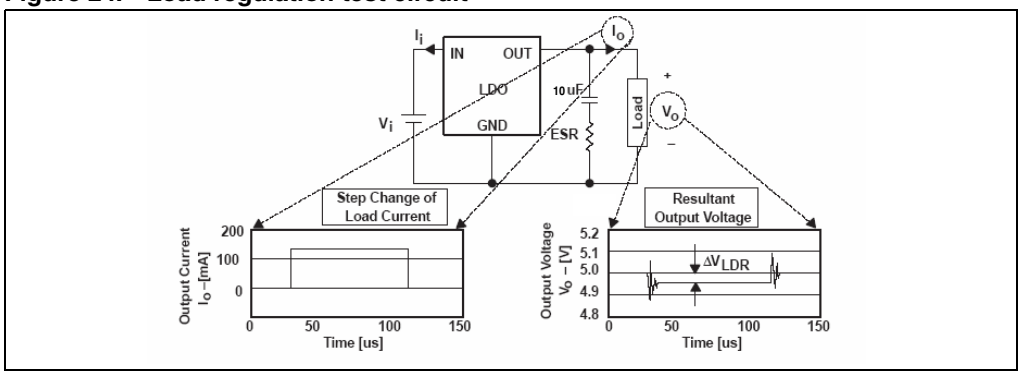
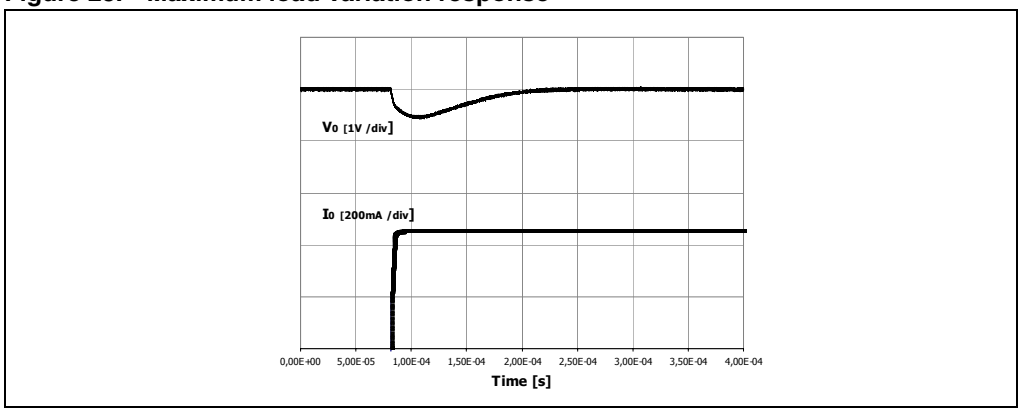
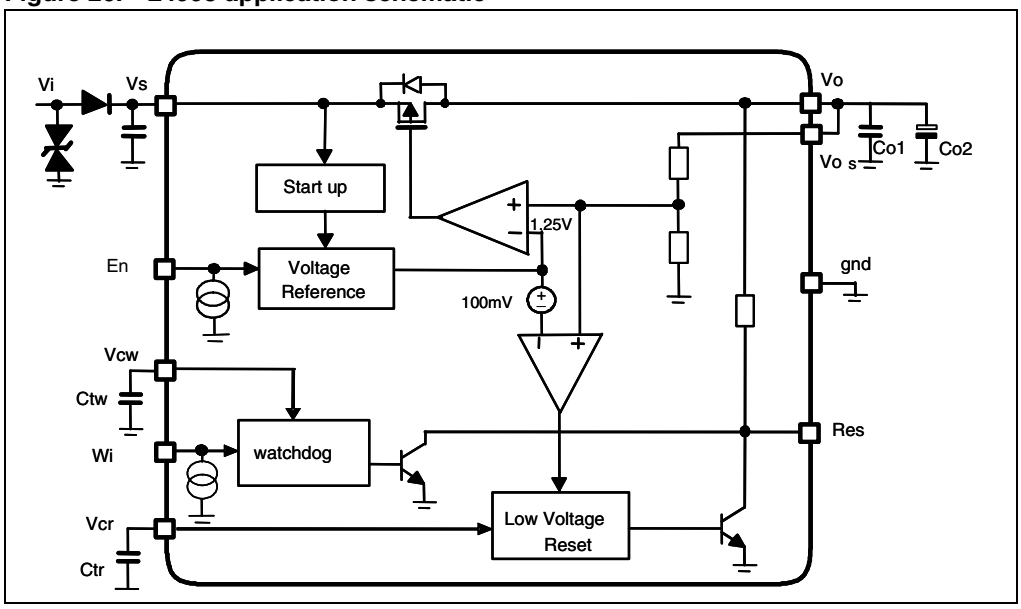


Figure 25. Maximum load variation response



3 Application information

Figure 26. L4995 application schematic



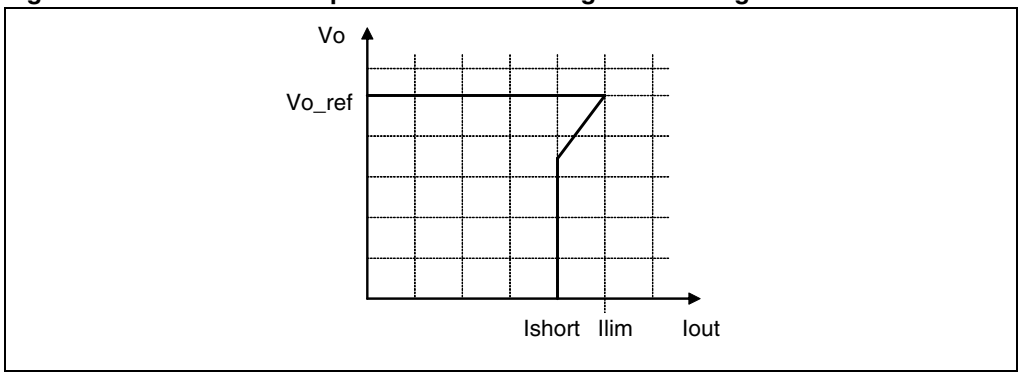
Note: The input capacitor Cs > 200nF is necessary for the smoothing of line disturbances. The output capacitor C01 > 100nF is necessary for the stability of the regulation loop. In order to dampen output voltage oscillations during high load current surges, it is recommended an additional electrolytic capacitor C02 > 10µF to be placed at the output pin.

3.1 Voltage regulator

Voltage regulator uses a p-channel transistor as a regulating element. With this structure, very low dropout voltage at current up to 500mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. A short circuit protection to GND is provided.

The voltage regulator is active when En is high.

Figure 27. Behavior of output current versus regulated voltage Vo



3.2 Reset

The reset circuit supervises the output voltage Vo. The Vo_th reset threshold is defined with the in-ternal reference voltage and a resistor output divider. If the output voltage becomes lower than Vo_th then Res goes low with a reaction time trr. The reset low signal is guaranteed for an output voltage Vo greater than 1V.

When the output voltage becomes higher than Vo_th then Res goes high with a delay trd. This delay is obtained by an internal oscillator.

The oscillator period is given by:

Tosc = [(Vrhth-Vrlth) x Ctr] / Icr + [(Vrhth-Vrlth) x Ctr] / Idr

where:

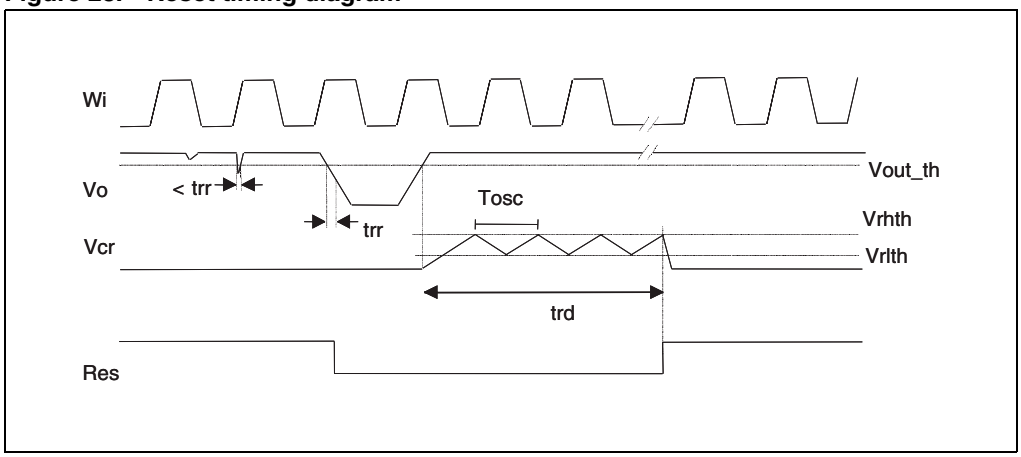
- Icr: is an internally generated charge current
- Idr: is an internally generated discharge current
- Vrhth, Vrlth: are two voltages defined with the output voltage and a resistor output divider
- Ctr: is an external capacitance.

trd is given by:

trd = (Vrhth x Ctr)/Icr + 3 x Tosc

Reset is active when En is high.

Figure 28. Reset timing diagram



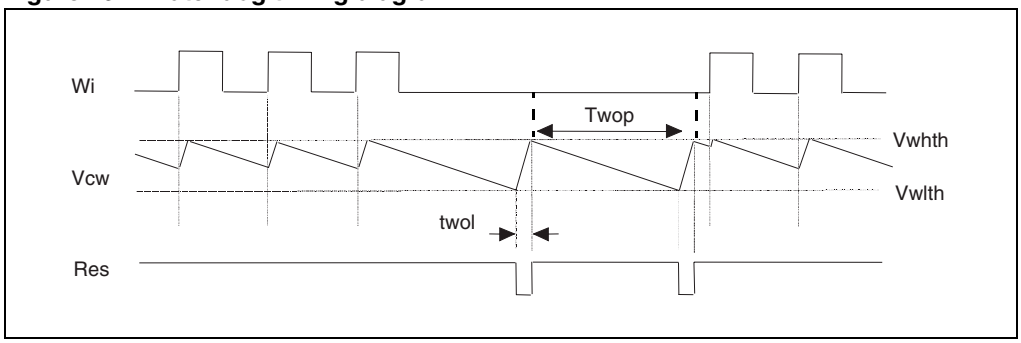
3.3 Watchdog

A connected microcontroller is monitored by the watchdog input Wi. If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor, Ctw. The watchdog circuit discharges the capacitor Ctw, with the constant current Icwd. If the lower threshold Vwlth is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold Vwlth. In order to calculate the minimum time t, during which the micro-controller must output the positive edge, the following equation can be used:

(Vwhth-Vwlth) x Ctw = Icwd x t

Every Wi positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, Vwhth, the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor Ctw.

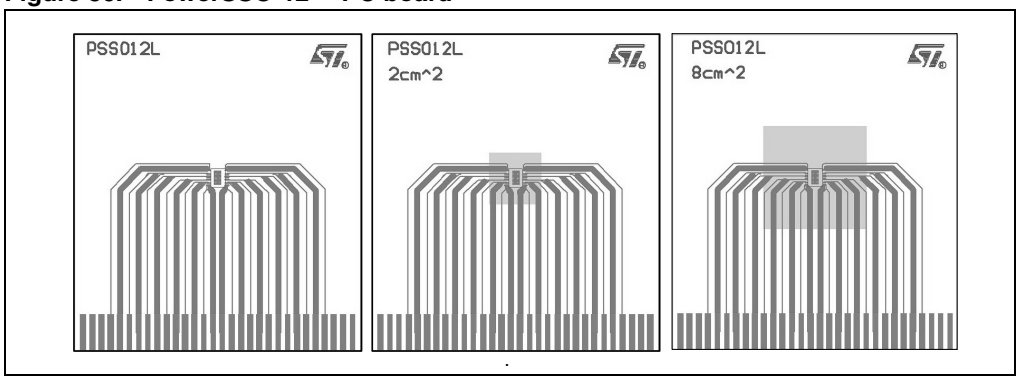
Figure 29. Watchdog timing diagram



4 Package and PCB thermal data

4.1 PowerSSO-12™ thermal data

Figure 30. PowerSSO-12™ PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm,PCB thickness=1.6mm, Cu thickness=70µm (front and back side) Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, Footprint dimension 4.1 mm x 6.5 mm).

Figure 31. $R_{thj\text{-}amb}$ Vs. PCB copper area in open box free air condition

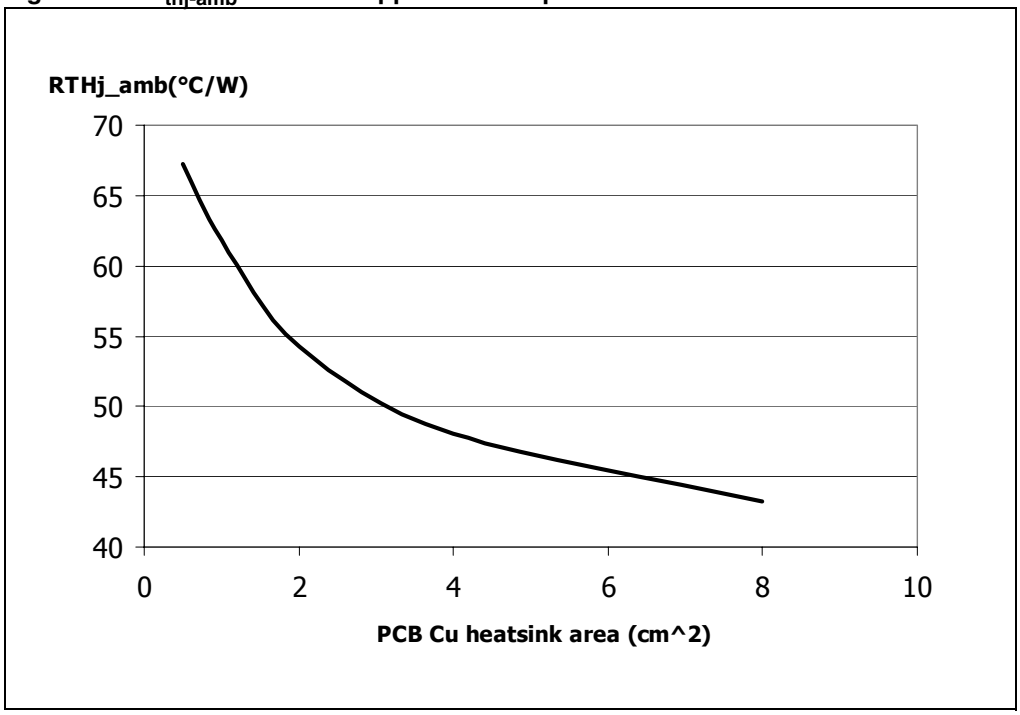
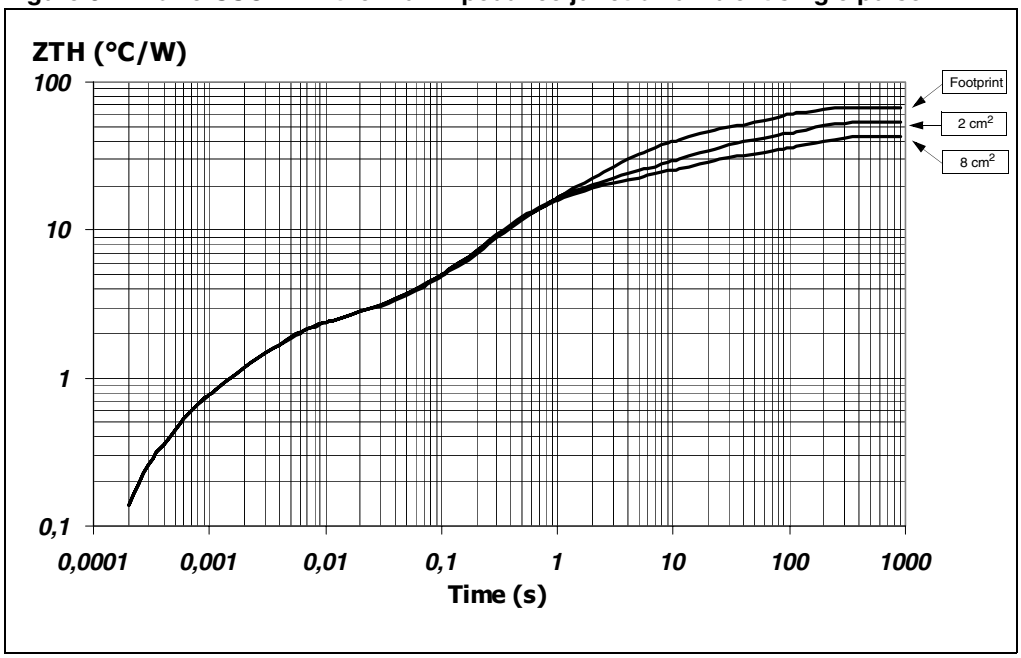


Figure 32. PowerSSO-12™ thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 33. Thermal fitting model of Vreg in PowerSSO-12™

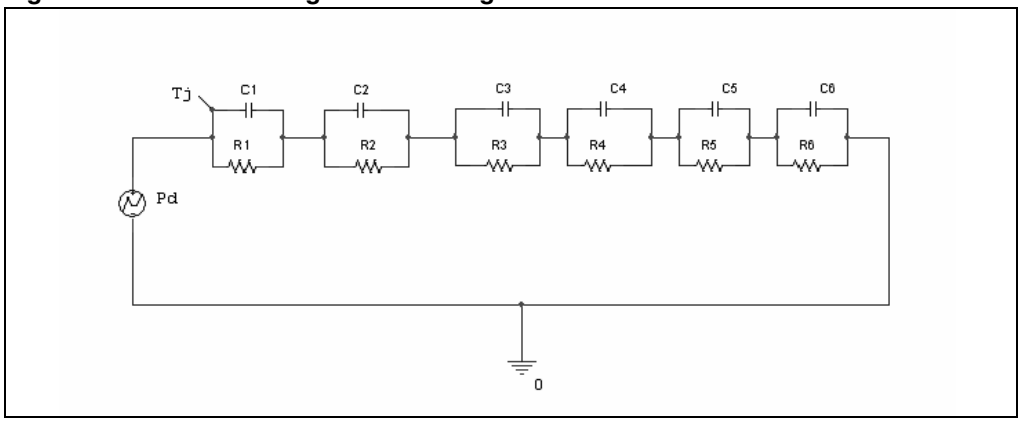
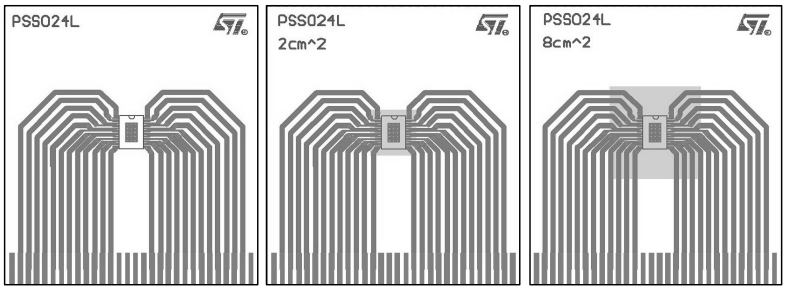


Table 9. PowerSSO-12™ thermal parameter

Area/island (cm^2)	Footprint	2	8
R1 (°C/W)	0.45		
R2 (°C/W)	1.79		
R3 (°C/W)	7		
R4 (°C/W)	10	10	9
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

4.2 PowerSSO-24™ thermal data

Figure 34. PowerSSO-24™ PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm,PCB thickness=1.6mm, Cu thickness=70µm (front and back side) Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, Footprint dimension 4.1 mm x 6.5 mm).

Figure 35. $R_{thj\text{-}amb}$ Vs. PCB copper area in open box free air condition

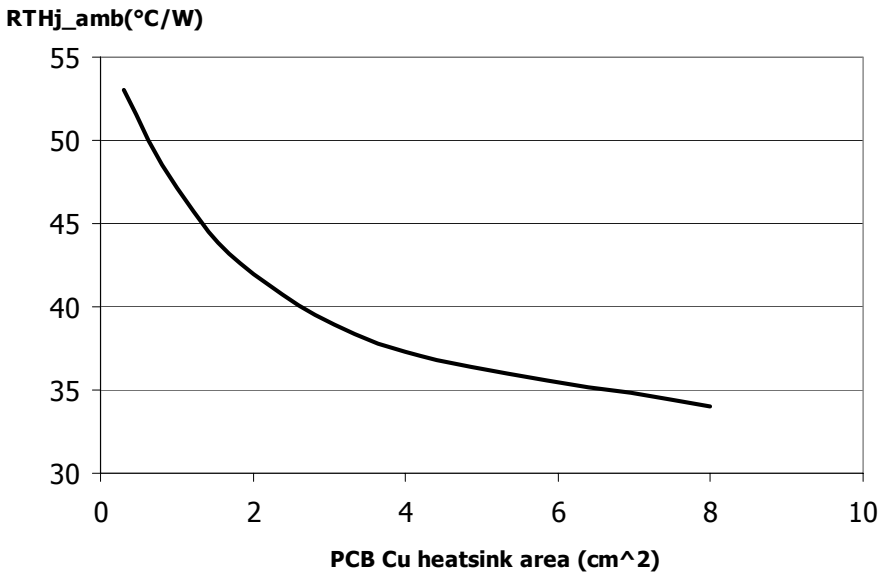
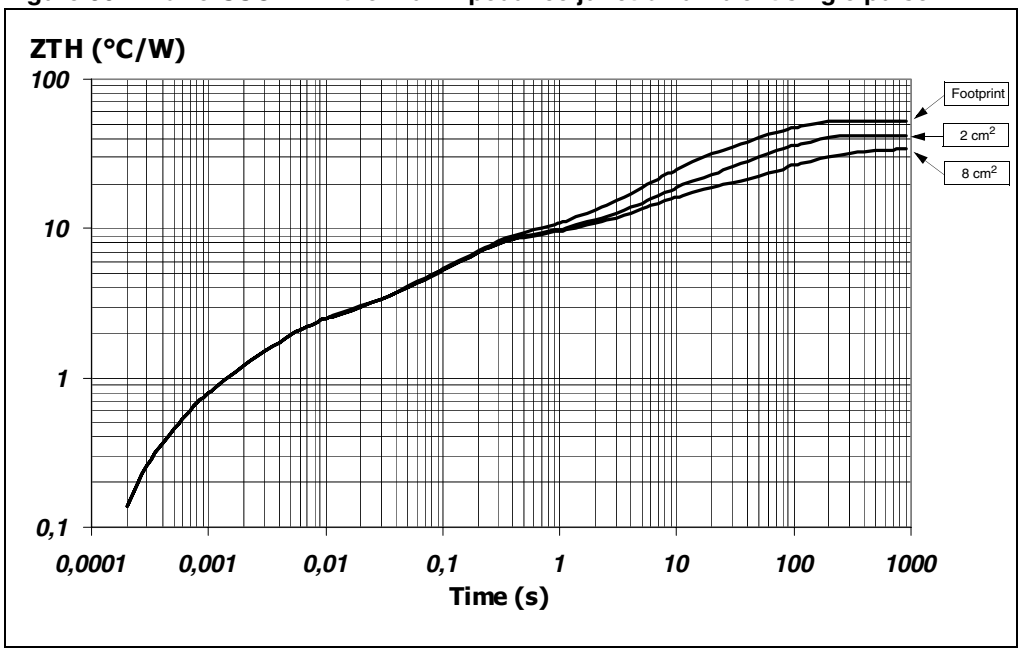


Figure 36. PowerSSO-24™ thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_P/T$

Figure 37. Thermal fitting model of Vreg in in PowerSSO-24™

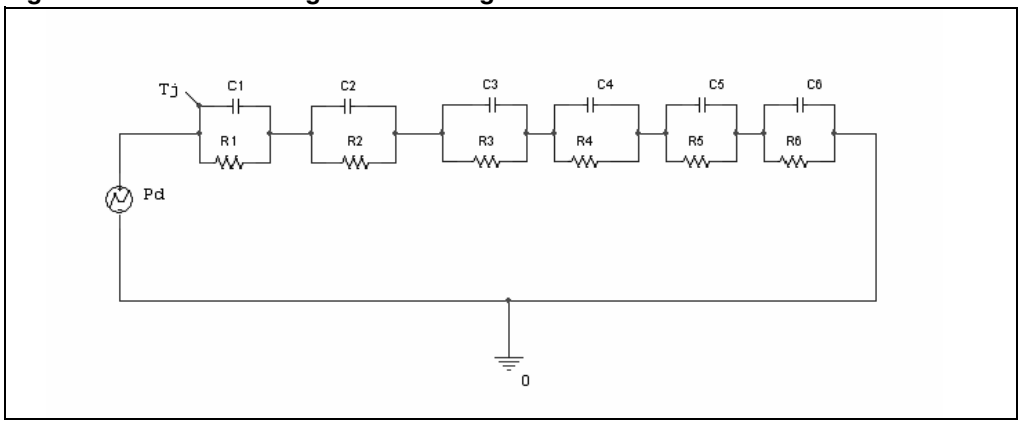


Table 10. PowerSSO-24™ thermal parameter

Area/island (cm^2)	Footprint	2	8
R1 (°C/W)	0.45		
R2 (°C/W)	1.79		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 38. PowerSSO-12™ package dimensions

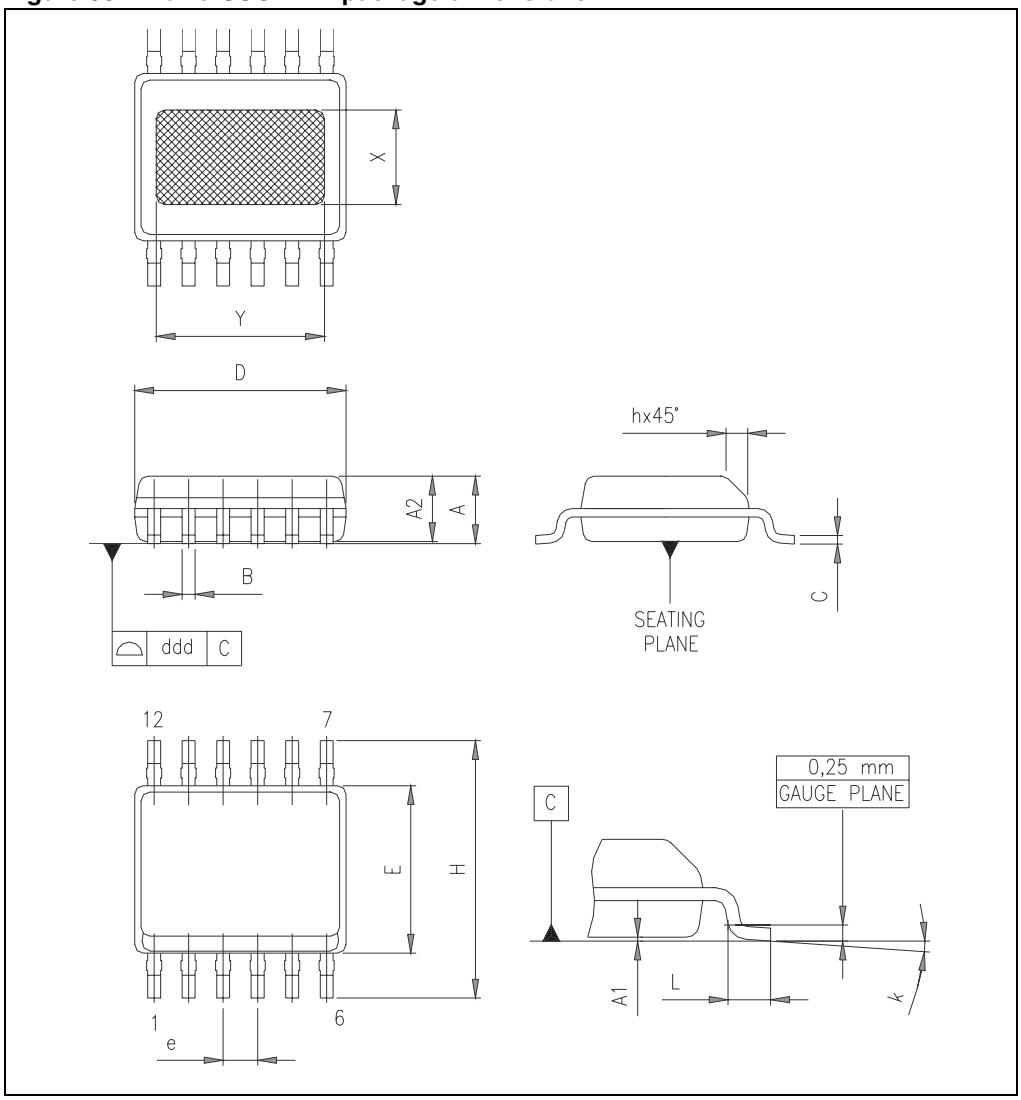


Table 11. PowerSSO-12™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0º		8º
X	2.200		2.800
Y	2.900		3.500
ddd			0.100

Figure 39. PowerSSO-24™ package dimensions

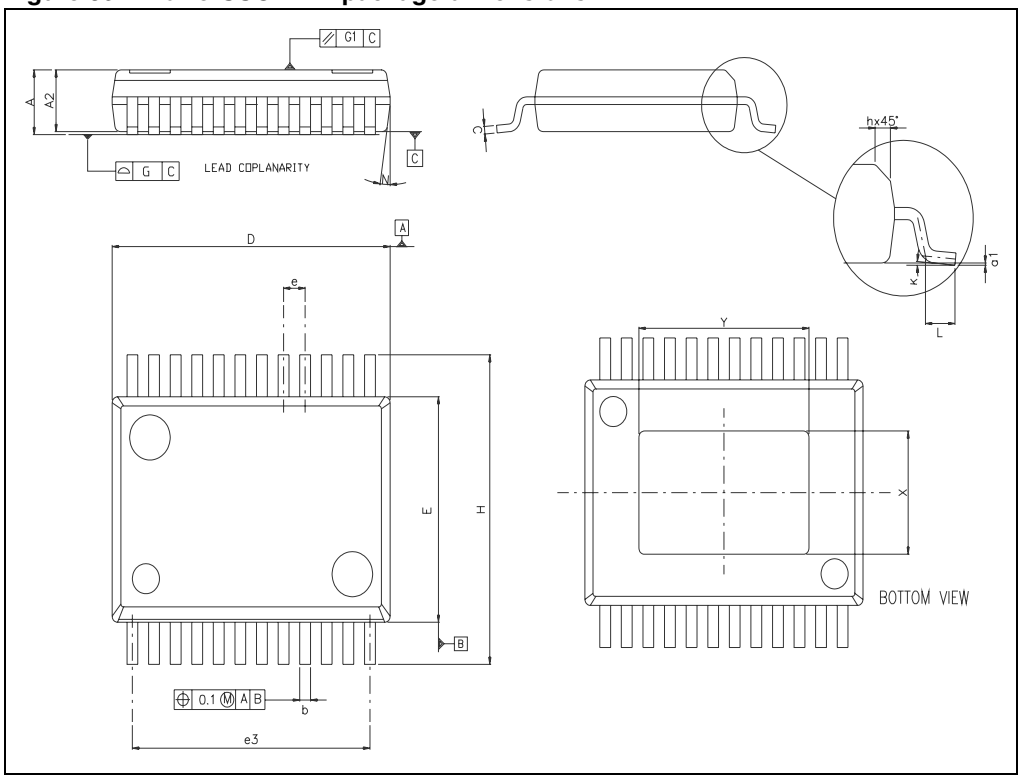


Table 12. PowerSSO-24™ mechanical data

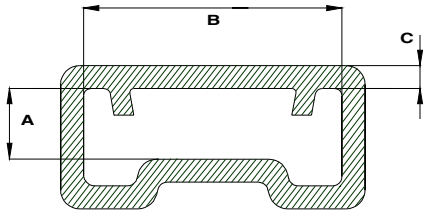
Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.1		10.5
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1

Table 12. PowerSSO-24™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
G1			0.06
H	10.1		10.5
h			0.4
k		5°	
L	0.55		0.85
N			10°
X	4.1		4.7
Y	6.5		7.1

5.2 PowerSSO-12™ packing information

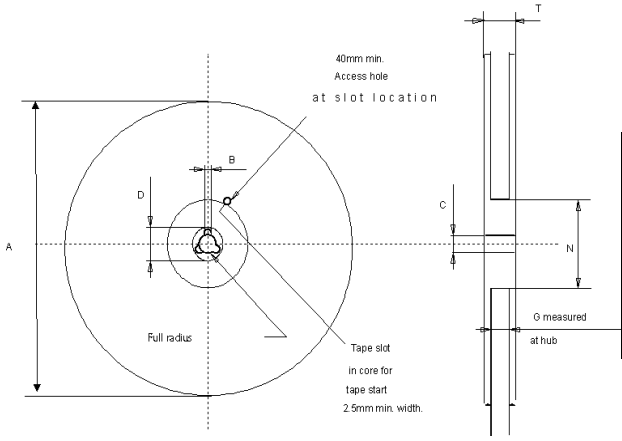
Figure 40. PowerSSO-12™ tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

All dimensions are in mm.

Figure 41. PowerSSO-12™ tape and reel shipment (suffix "TR")



REEL DIMENSIONS

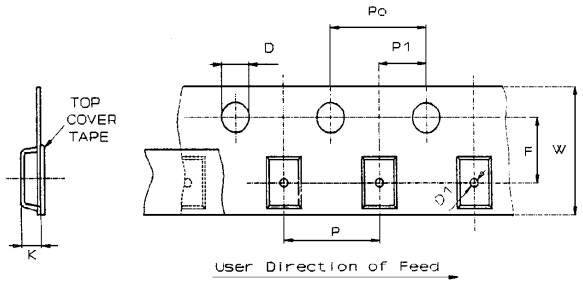
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

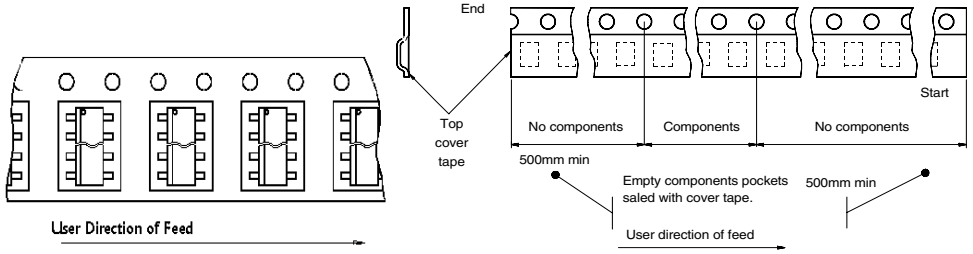
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D (± 0.05)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.1)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

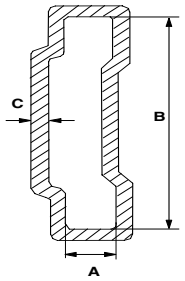
All dimensions are in mm.





5.3 PowerSSO-24™ packing information

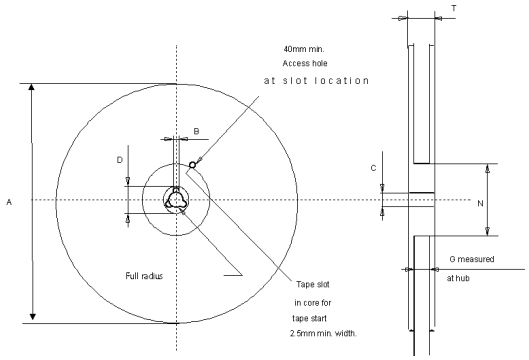
Figure 42. PowerSS0-24™ tube shipment (no suffix)



Base Qty	49
Bulk Qty	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

All dimensions are in mm.

Figure 43. PowerSSO-24™ tape and reel shipment (suffix "TR")



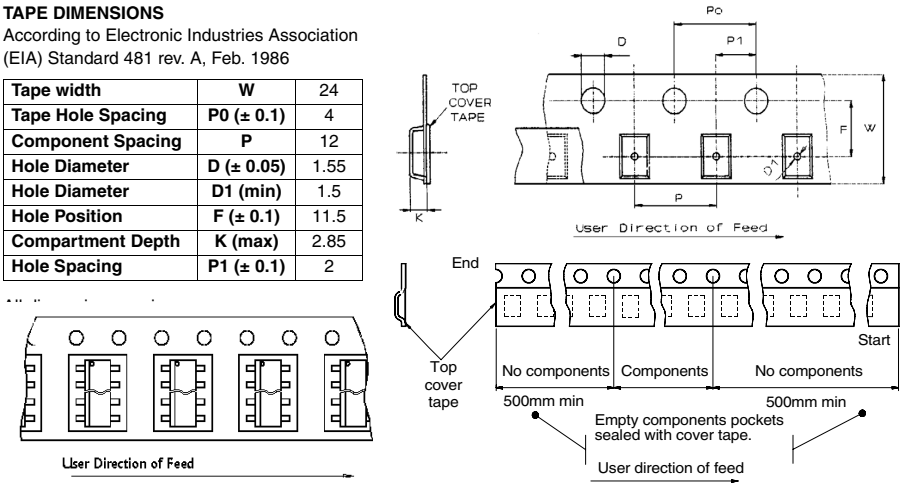
REEL DIMENSIONS

Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (± 0.1)**	2



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
26-May-2006	1	Initial release.
05-Jan-2007	2	L4995A and L4995R versions added: *Features* section updated and table added. *Table 1: Device summary* updated. *Table 5: Electrical characteristics*, Watchdog Iwi entry updated. *Figure 2: Block diagram of L4995A* and *Figure 3: Block diagram of L4995R* added. *Table 2: Pins descriptions* updated. *Table 4: Thermal data* updated. *List of tables* and *List of figures* added. Packaging information provided in new format. *Table 11: PowerSSO-12™ mechanical data* X and Y values updated. Some sections reformatted for clarity. New disclaimer added.
18-May-2007	3	Updated *Table 2: Pins descriptions*. Updated *Figure 4: Pins configurations (L4995)*. *Table 1* changed title.
09-Jul-2007	4	Updated *Table 2: Pins descriptions*.

Table 13. Document revision history (continued)

Date	Revision	Changes
09-Aug-2007	5	Updated *Table 2: Pins descriptions*. Updated *Table 12: PowerSSO-24™ mechanical data*.
07-Dec-2007	6	Updated *Section 2.2: Thermal data*: – corrected note changing single layer with double layer. Updated *Table 5: General*: – changed I_{short} typ. value from 750 to 800 mA – added I_{short} max. value – changed I_{lim} typ. value from 820 to 900 mA – added I_{lim} max. value – added I_{lim} note – added V_{dp} note – changed I_{qn_1} typ. value from 110 to 90 µA – added I_{qn_1} max. value – added I_{qn_50} max. value – added I_{qn_150} max. value – changed I_{qn_250} typ. value from 1.2 to 1 mA – added I_{qn_250} max. value – changed I_{qn_500} typ. value from 2.4 to 2.1 mA – added I_{qn_500} max. value Updated *Table 6: Reset*: – changed Vrlth parameter definition from “Reset timing low” to “Reset delay circuit low threshold” – changed Vrhth parameter definition from “Reset timing high” to “Reset delay circuit high threshold” – added Trd min. and max. values Updated *Table 7: Watchdog*: – added Iwi max value Updated *Table 8: Enable*: – changed Pull down current symbol from $R_{En\ to}\ I_{En}$ – changed I_{En} typ. value from 2.5 to 10 µA – added I_{En} max. value Added *Section 2.4: Electrical characteristics curves*. Added *Section 2.5: Test circuit and waveforms plot*. Added *Section 4: Package and PCB thermal data*

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